JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA

Results for M.Tech II SEMESTER (R16 / R13) Regular / Supplementary Examinations , JUNE- 2018 .

College: ADITYA ENGG. COLLEGE, SURAMPALEM, PEDDAPURAM:A9

Discrepancy pertaining to these results are to be submitted on or before 24-09-2018 with following documents at CE(PG) Office,JNTUK,Kakinada

Htno	Subcode	Subname	Internal	External	credits
14A91D0405	H0402	COMPUTER GRAPHICS	26	30	1
14A91D0405	H2103	FINITE ELEMENT METHOD	26	10	0
14A91D0817	H0802	ARTIFICIAL LIFT TECHNIQUES	33	16	0
14A91D0817	H0803	OPERATIONAL ASPECTS OF WELL TESTING	34	6	0
14A91D0817	H0804	INTEGRATED RESERVOIR MANAGEMENT	38	0	0
14A91D0817	H0807	FLOW ASSURANCE	39	6	0
14A91D2108	H2109	THERMAL MEASUREMENTS AND PROCESS CONTROL	26	27	1
14A91D2109	H2103	FINITE ELEMENT METHOD	27	0	0
14A91D2117	H2104	COMPUTATIONAL FLUID DYNAMICS	26	24	1
14A91D5204	H4301	SWITCHED MODE POWER CONVERSION	27	-1	0
14A91D5206	H4301	SWITCHED MODE POWER CONVERSION	29	26	1
14A91D5509	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	34	26	1
14A91D5511	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	27	5	0
15A91D2102	H2104	COMPUTATIONAL FLUID DYNAMICS	27	34	1
15A91D2102	H2109	THERMAL MEASUREMENTS AND PROCESS CONTROL	33	37	1
15A91D2106	H2104	COMPUTATIONAL FLUID DYNAMICS	31	33	1
15A91D5203	H4301	SWITCHED MODE POWER CONVERSION	35	15	0
15A91D5501	H5502	EMBEDDED NETWORKING	37	26	1
15A91D5501	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	24	1
15A91D5504	H4508	INTERNET PROTOCOLS	30	20	0
15A91D5504	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	36	0	0
15A91D5507	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	35	0	0
15A91D5509	H6805	DIGITAL SIGNAL PROCESSORS & ARCHITECTURE	35	12	0
16A91D2102	J2101	FUELS COMBUSTION & ENVIRONMENT	30	34	1
16A91D2102	J2104	COMPUTATIONAL FLUID DYNAMICS ELECTIVE-II	31	14	0
16A91D2104	J2101	FUELS COMBUSTION & ENVIRONMENT	30	31	1
16A91D2105	J2101	FUELS COMBUSTION & ENVIRONMENT	32	43	1
16A91D2105	J2103	FINITE ELEMENT METHODS	36	28	1
16A91D2106	J2103	FINITE ELEMENT METHODS	34	24	1
16A91D2106	J2104	COMPUTATIONAL FLUID DYNAMICS ELECTIVE-II	31	15	0
16A91D5501	J5501	HARDWARE SOFTWARE CODESIGN	27	9	0
16A91D5501	J5702	SYSTEM ON CHIP DESIGN ELECTIVEIV	28	30	1
16A91D5501	J6802	CMOS MIXED SIGNAL CIRCUIT DESIGN	23	21	0
16A91D5501	J6805	DSP PROCESSORS AND ARCHITECTURES	24	3	0
16A91D5501	J6809	CPLD AND FPGA ARCHITECTURES AND APPLICAT	25	18	0
16A91D5506	J5702	SYSTEM ON CHIP DESIGN ELECTIVEIV	33	40	1
16A91D5803	J0502	SOFTWARE ENGINEERING ELECTIVE I	26	26	1
16A91D5803	J2503	CYBER SECURITY	30	5	0
16A91D5803	J2510	CLOUD COMPUTING ELECTIVE II	27	13	0
16A91D5803	J4001	ADVANCED UNIX PROGRAMMING	28	0	0
16A91D5803	J4002	BIG DATA ANALYTICS	28	6	0

Htno	Subcode	Subname	Internal	External	credits
16A91D5803	J5801	COMPUTER NETWORKS	33	4	0
16A91D5804	J2503	CYBER SECURITY	35	26	1
16A91D5804	J4002	BIG DATA ANALYTICS	36	24	1
16A91D5805	J5801	COMPUTER NETWORKS	39	34	1
16A91D7202	J6804	DESIGN FOR TESTABILITY	36	28	1
16A91D8704	J8704	THEORY OF PLATES & SHELLS	37	30	1
16A91D8704	J8705	PRESTRESSED CONCRETE ELECTIVEI	38	36	1
16A91D8705	J8705	PRESTRESSED CONCRETE ELECTIVEI	37	31	1

**Note:1)For Recounting/Revaluation/Challenge By Revaluation Apply through Online(www.jntukresults.edu.in))

NOTE:2 [Last Date for Apply Recounting/Revaluation/Challenge By Revaluation: **01-10-2018]

**NOTE:3 [Please inform to the students to enter these subject codes for applying Recounting/Revaluation/Challenge By Revaluation]

**NOTE:
[-1 in the filed of externals indicates student absent for the respective subject.

-2 in the filed of externals indicates student result is withheld for the respective subject.

-3 in the filed of externals indicates Malpractice for the respective subject.]

N. Mohan Rao

Date:17-09-2018

Controller of Examinations